Surface Mount 10 W High Power Amplifier 17-20.5 GHz

ReliaSat

Product Datasheet

HPA11201721QF

Surface Mount 10 W GaN MMIC High Power Amplifier for K-band.

Overview

HPA11201721QF is a High Power MMIC Amplifier fabricated on Space Qualified 0.25 um GaN on SiC. This MMIC operates from 17-20.5 GHz and delivers >10 W saturated output power across the band, with power-added efficiency in excess of 25% and large-signal gain of 20 dB.

The part is offered in a 7x7 mm hermetically sealed surface mount ceramic package and is matched to 50 Ω with integrated DC blocking capacitors on RF ports. The part incorporates an output power detector to assist with system integration and is well suited for satellite communications and point to point applications.

Features

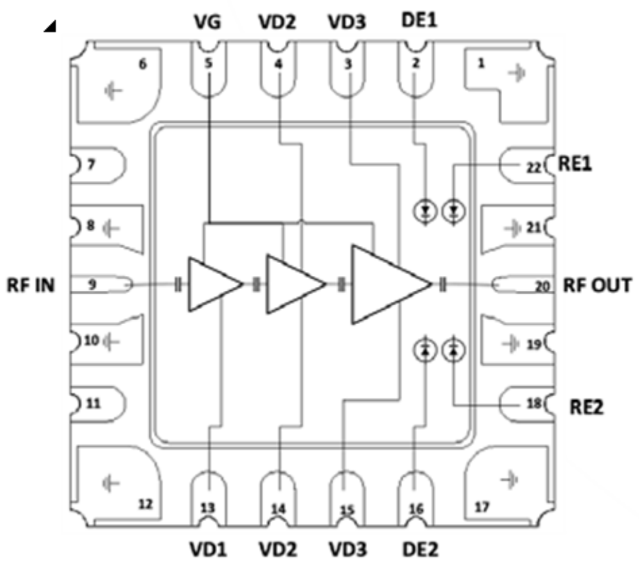
- Frequency range 17-20.5 GHz
- Power >10 W saturated
- Small signal gain 25 dB
- Large signal gain 20 dB
- Integrated power detector
- PAE: >25% at Pin=20 dBm
- Bias: VD=25 V, IDQ=300 mA, VG-3.6 V
- QFN dimensions 7x7 mm

Applications

- Satellite communications
- Radar
- Mobile communications
- 5G

Available as	
HPA11201721B	17-20.5 GHz bare die GaN HPA
HPA11201721BE	17-20.5 GHz bare die GaN HPA evaluation board
HPA11201721QF	17-20.5 GHz packaged GaN HPA
HPA11201721QFE	17-20.5 GHz packaged GaN HPA evaluation board
SSPA11201721SS	17-20.5 GHz GaN solid state power amplifier

Functional Diagram



Electrical Specification

Freq 17-20.5 GHz, T_a=25 °C V_d=25 V, Idq=300 mA, Zo=50 Ω

Parameter	Test Conditions	Min	Typ	High	Unit
Operational Frequency Range		17.0		20.5	(GHz)
Small Signal Gain	17-19 GHz 19-20.5 GHz		25 22		(dB)
Input Return Loss	17.5-20.5 GHz		10		(dB)
Output Return Loss	17.5-20.5 GHz		10		(dB)
Output Power at Saturation	17.5-19.5 GHz 19.5-20.5 GHz		42 40		(dBm)
Power Added Efficiency	Pin=20 dBm 17.5-19 GHz 19-20 GHz 20.5 GHz		33 25 20		(%)
Output Power Temperature Coefficient	19 GHz, Psat -40 to 85 °C		0.03		(dB/°C)

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage (V_d)	30 V
Gate Voltage Range (V_g)	-8 to 0 V
Drain Current (I_d)	2.5 A
Power Dissipation (PDISS) 85 °C	44 W
Input Power (Pin)	23 dBm
Mounting Temperature (30 seconds)	260 °C
Storage Temperature	-55 to 150 °C
Junction Temperature	200 °C

Exceeding any one or combination of these limits may cause permanent damage to this device. Sustained operation near these survivability limits is not recommended.

Recommended Operating Conditions

Parameter	Rating
Drain Voltage (V_d)	20-30 V
Gate Voltage Range (V_g)	-3.6 (TYP)
Drain Current, Quiesent (I_{dq})	300 mA
Junction Temperature	<200 °C

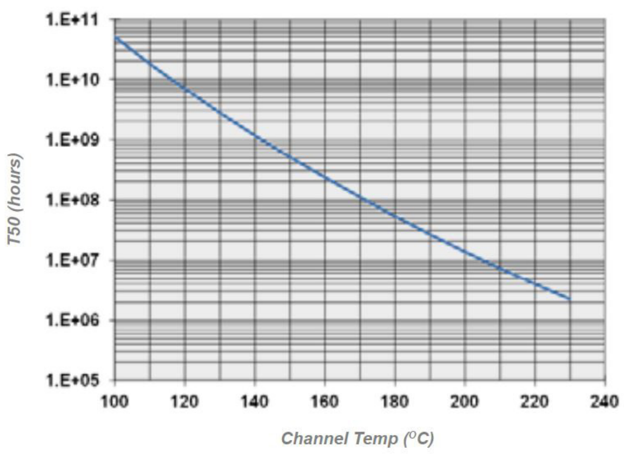
Thermal Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θjc)[1]	Tbase= 85 °C, V_d=25 V, I_d=0-1.5 A	2.62	°C/W

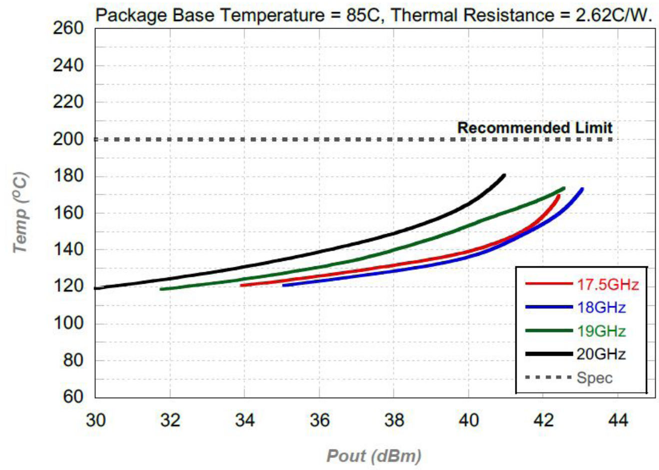
Notes:
Thermal resistance measured using Raman Thermography on device channel referenced to back of package.

Median Time To Failure vs Channel Temperature

0.25 um GaN process

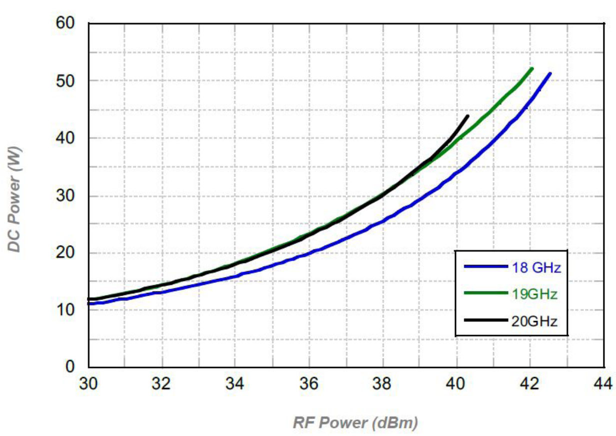


Channel Temperature vs Pout



Power Consumption

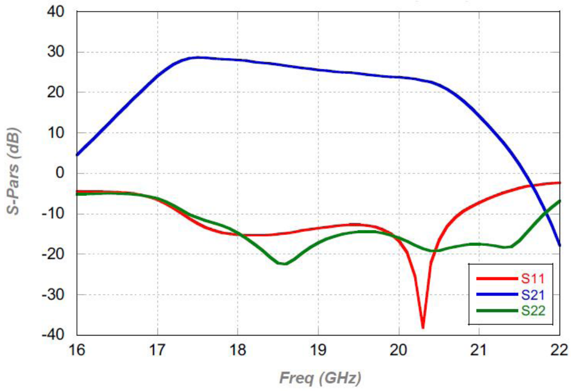
DC power consumption vs output power



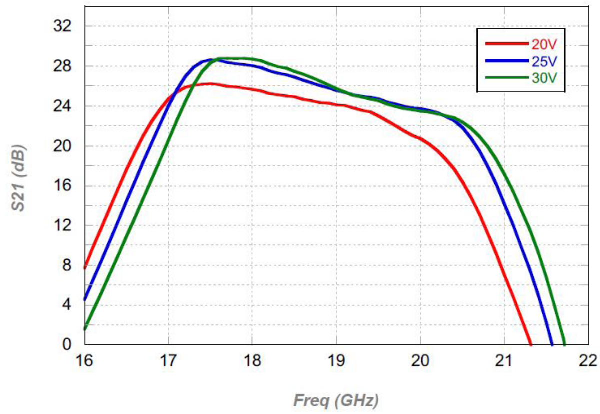
Small Signal Performance Curves

V_D=25 V, I_{DQ}=300 mA, V_G~-3.6 V typical, T_A=25 °C

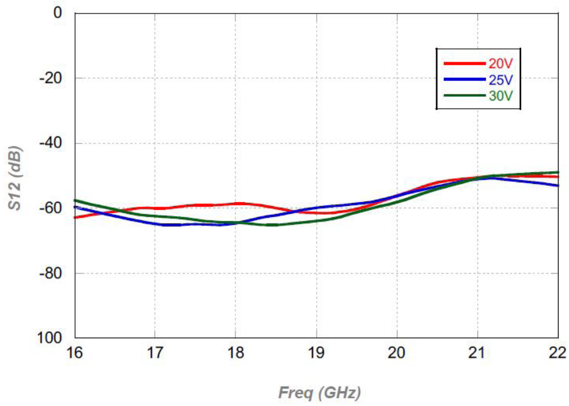
S-Parameters vs Frequency



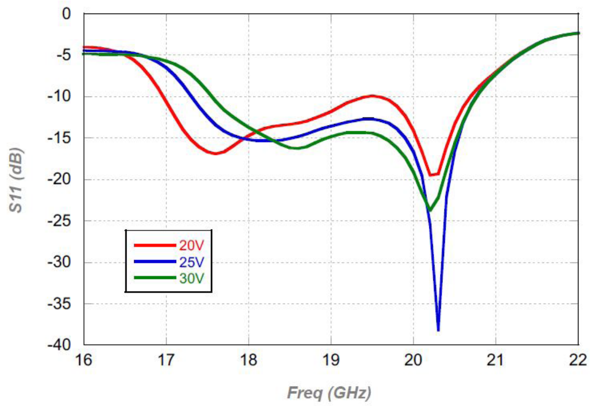
Small Signal Gain vs Frequency vs Drain Voltage



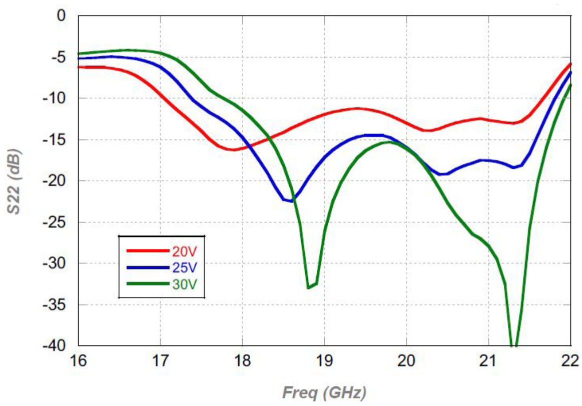
Reverse Gain vs Frequency vs Drain Voltage



Input Return Loss vs Frequency vs Drain Voltage



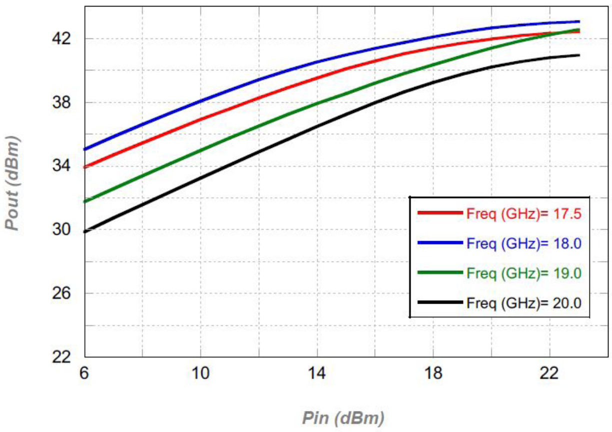
Output Return Loss vs Frequency vs Drain Voltage



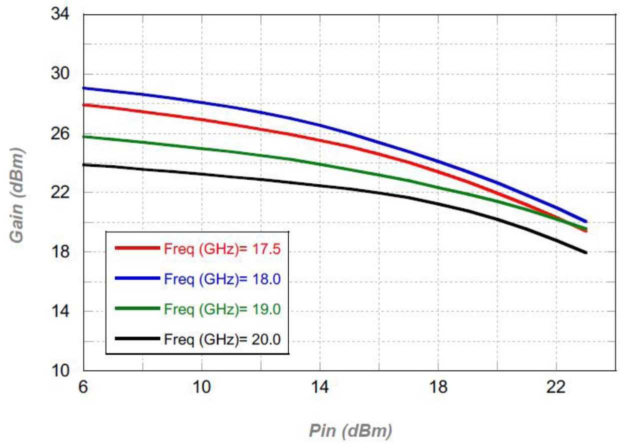
Large Signal Performance Curves

V_D=25 V, I_{DQ}=300 mA, V_G~-3.6 V typical, T_A=25 ^{O}C

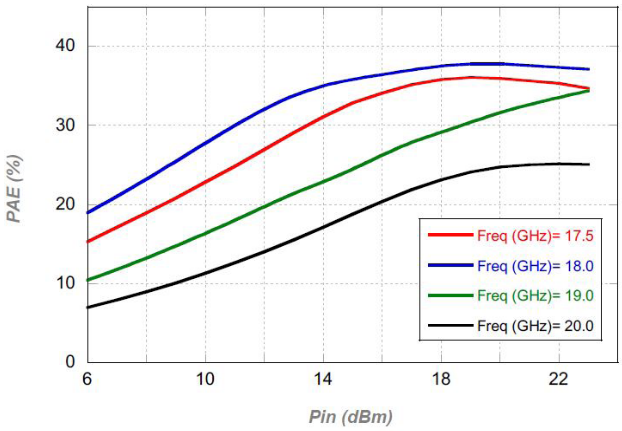
Pout vs Pin vs Frequency



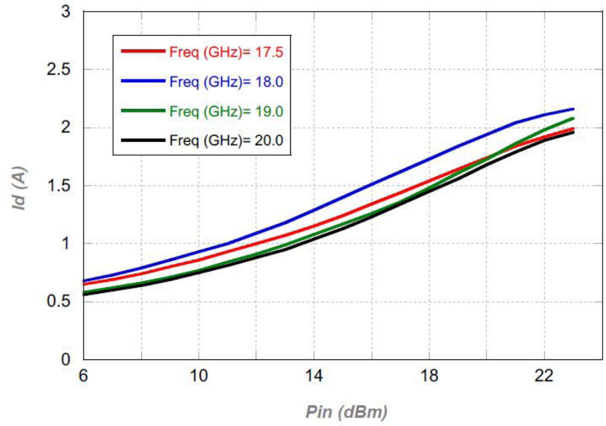
Gain vs Pin vs Frequency



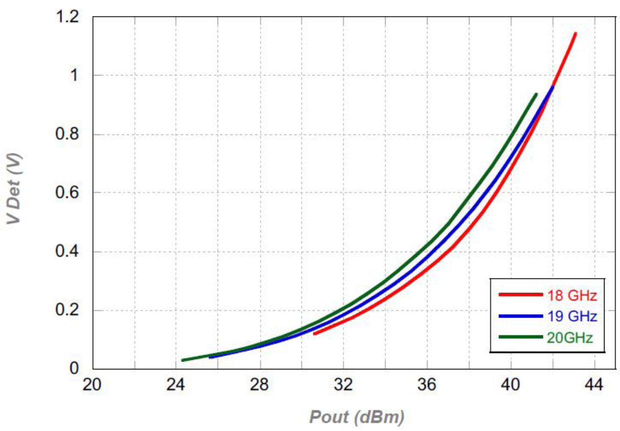
PAE vs Pin vs Frequency



Drain Current vs Pin vs Frequency



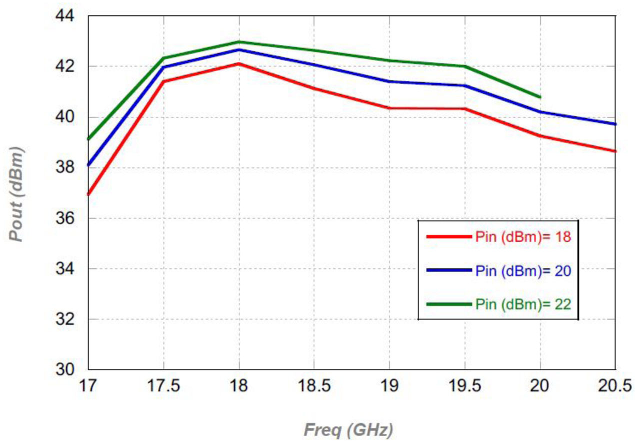
Power Detect Voltage vs Pout



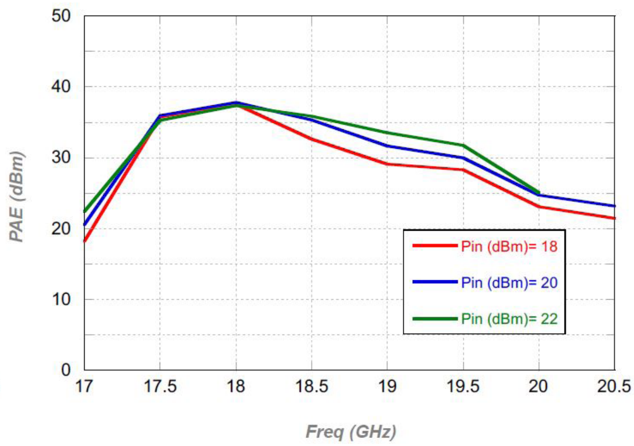
Large Signal Performance Curves

V_D=25 V, I_{DQ}=300 mA, V_G~-3.6 V typical, T_A=25 ^{O}C

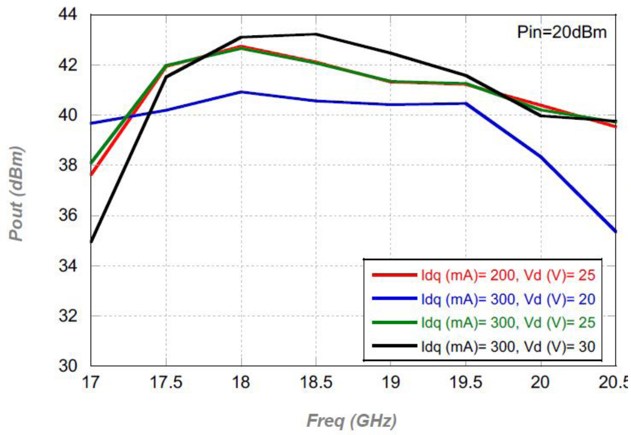
Pout vs Frequency vs Pin



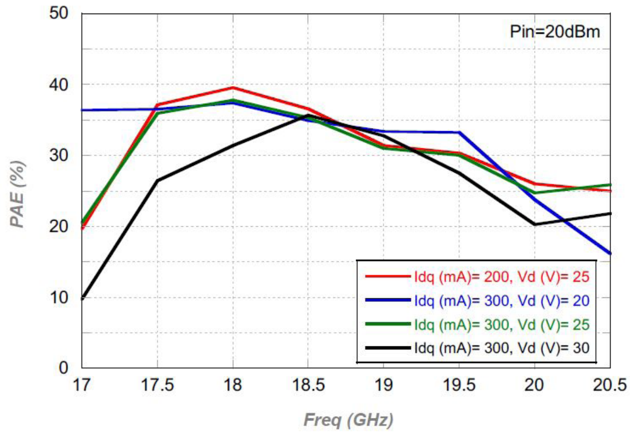
PAE vs Frequency vs Pin



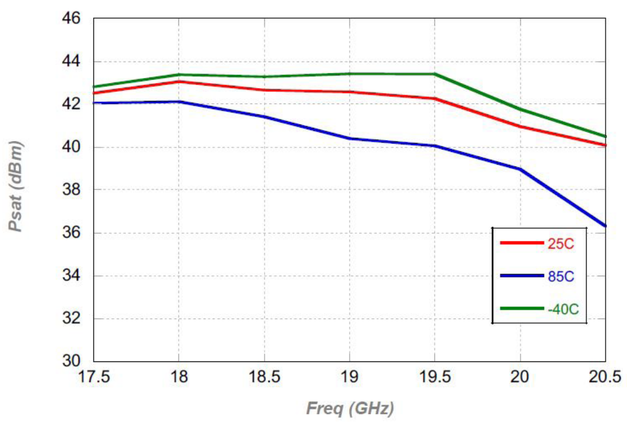
Pout vs Frequency vs Bias



PAE vs Frequency vs Bias



Saturated Power vs Frequency vs Temperature



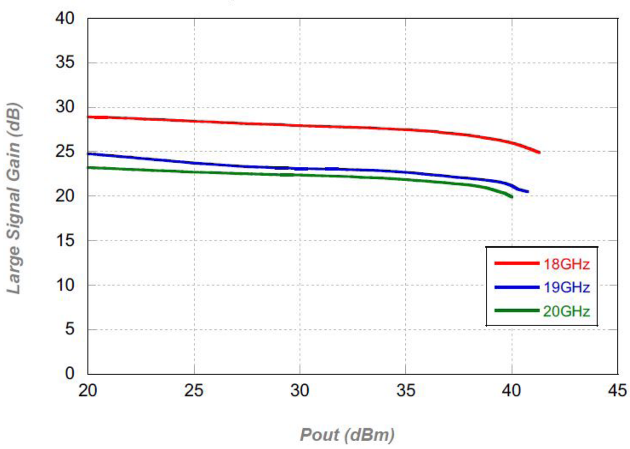
Surface Mount 10 W High Power Amplifier
17-20.5 GHz

Product Datasheet

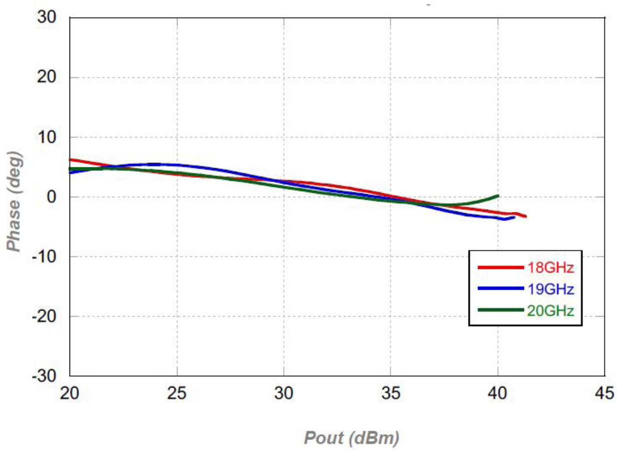
Linearity Performance Curves

V_D=25 V, I_{DQ}=300 mA, V_G~-3.6 V typical, T_A=25 ^oC

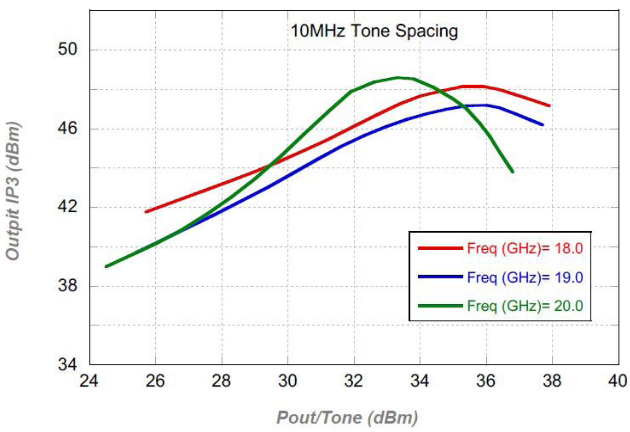
AM/AM vs Frequency



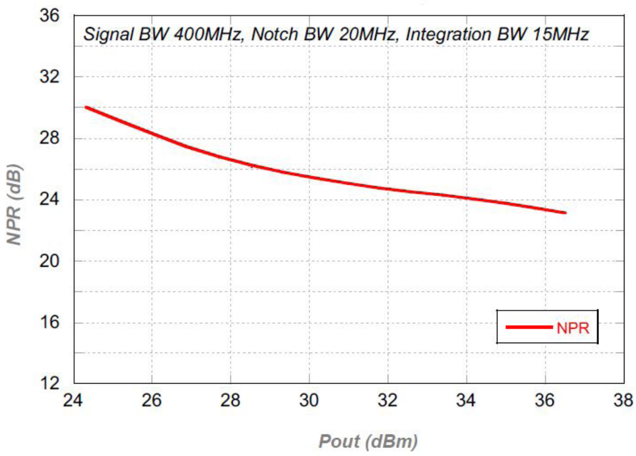
AM/PM vs Frequency



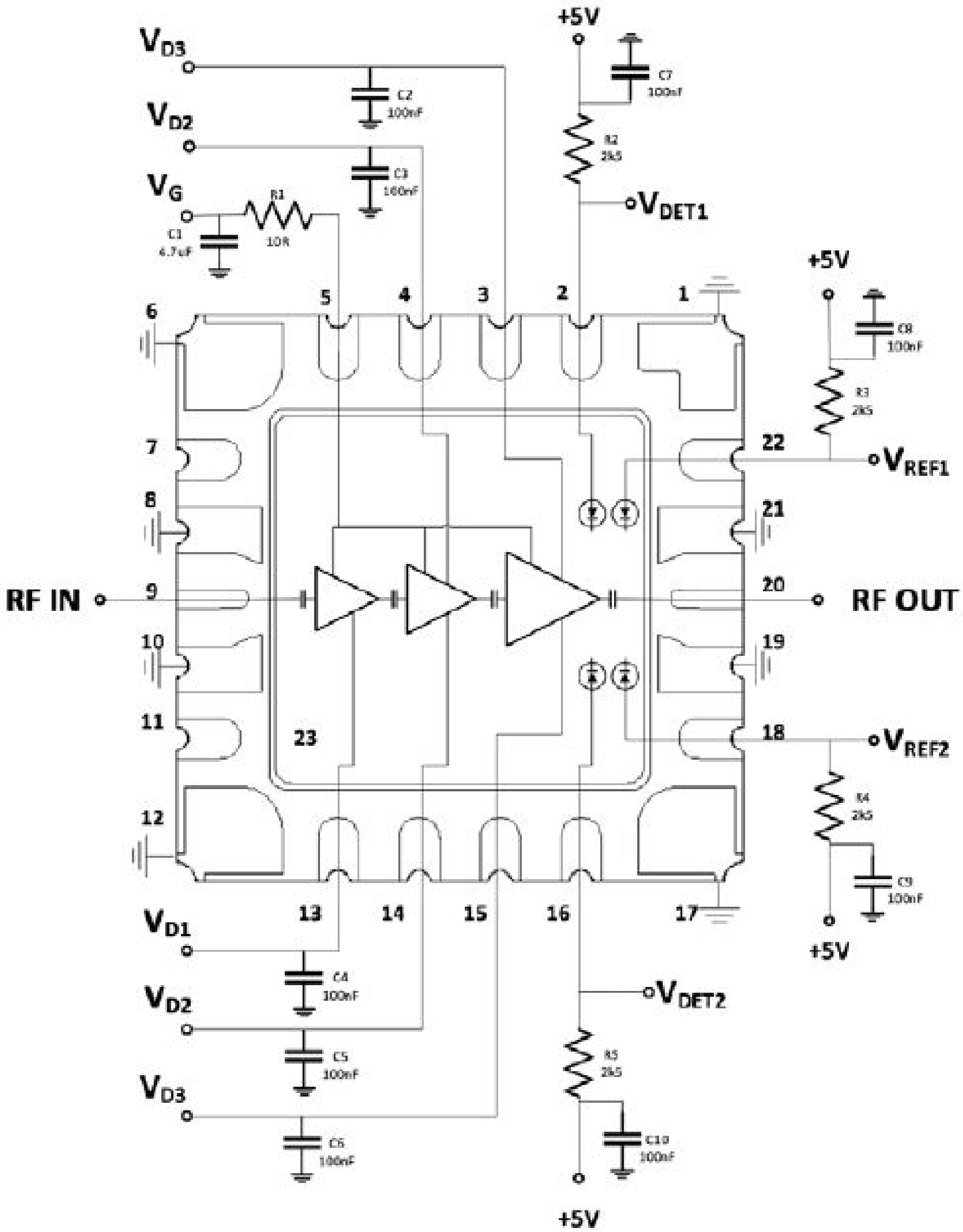
Output IP3 vs Pout/Tone vs Frequency



Noise Power Ratio vs Average Pout at 19 GHz



Recommended Application Circuit



Bill Of Materials

Part	Vale	Case Size
C1	4.7 uF	1608 (0603)
C2, C3, C4, C5. C6. C7, C8, C9 C10	100 nF	1608 (0603)
R1	10 Ohm	1005 (0402)
R2, R3, R4, R5	2.5k Ohm	1005 (0402)

Bias

Sequences

Bias Up Sequence	Bias Down Sequence
1. Set ID limit to 2.5 A, IG limit to 50 mA	1. Turn off RF supply
2. Apply -5 V to VG	2. Reduce VG to -5 V
3. Apply +25 V to VD; IDQ is ~0 mA	3. Set VD to 0 V
4. Adjust VG until IDQ = 300 mA (VG~ -3.6 V)	4. Turn off VD supply
5. Turn on RF supply	5. Turn off VG supply

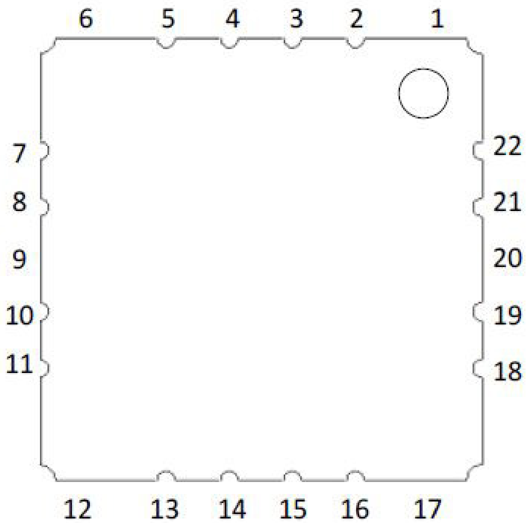
Arrangement

D2 and D3 must be biased from both sides.
Drain side capacitors should be 35 V minimum rating.
Bypass capacitors should be placed as close to the packaged device as possible.

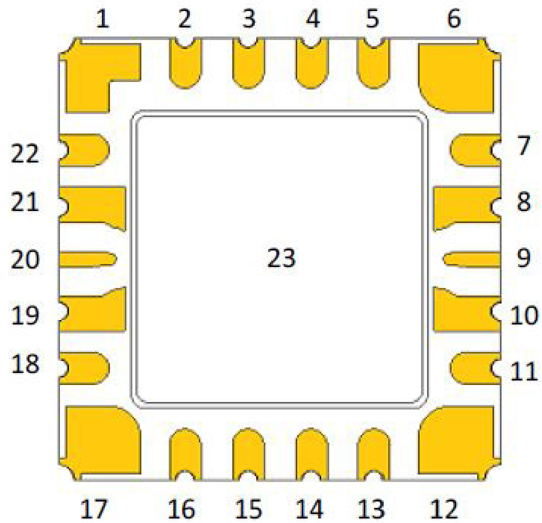
Detector Operation

HPA11201721QF includes power detectors on both sides of the device to facilitate integration into larger systems. The power detector requires an external 5V supply. For temperature compensation, the VDET and VREF outputs can be connected to a voltage comparator circuit, the output from which can be fed into an ADC or multimeter for the result.

Pin Descriptions

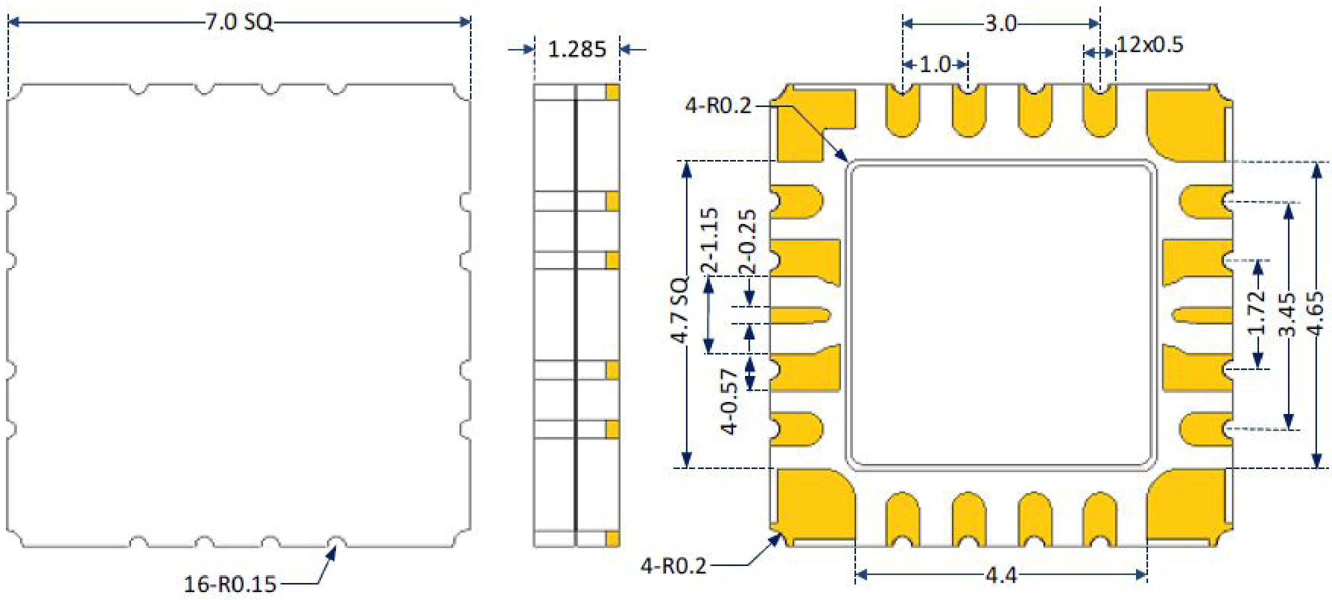


Top View



Bottom View

Pad Number	Label	Description
1, 6, 8, 10, 12, 17, 19, 21, 23	GND	Ground
2, 16	V_{DET}	Detector Diode Output Voltage
3, 15	$V_{D}3$	Drain Voltage Stage 3
4, 14	$V_{D}2$	Drain Voltage Stage 2
5	V_{G}	Gate Voltage (all stages)
7, 11	NC	No Connect
9	RF_{IN}	RF Input, 50 Ω matched, DC Blocked
13	$V_{D}1$	Drain Voltage Stage 1
18, 22	V_{REF}	Reference Diode Output Voltage
20	RF_{OUT}	RF Output, 50 Ω matched, DC Blocked



Units: mm
Tolerances ±0.15

Materials:
Package: Metal/Ceramic
Lid: Metal/Ceramic

Melted Au-Sn preform is bonded on the plated surface
Metal Finish: Ni PLATE + Au PLATE 1.0μmMIN.

General Notes On Assembly

1. Clean the board or module with alcohol and allow it to fully dry.
2. Apply solder paste to each pin and heat achieve re-flow, being careful not to exceed the thermal budget.
3. After completing the soldering process, allow the devices to cool naturally for at least 3 minutes.
4. Avoid any mechanical stress or shock to the solder joints and devices during cooling,
5. Clean the assembly with alcohol.

Solderability

Compatible with the latest version of J-STD-020, Lead-free solder, 260 ^{o}C

Handling Precautions

Parameter	Rating
ESD - Human Bodel Model (HBM)	TBD

CAUTION!
ESD – Sensitive Device

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

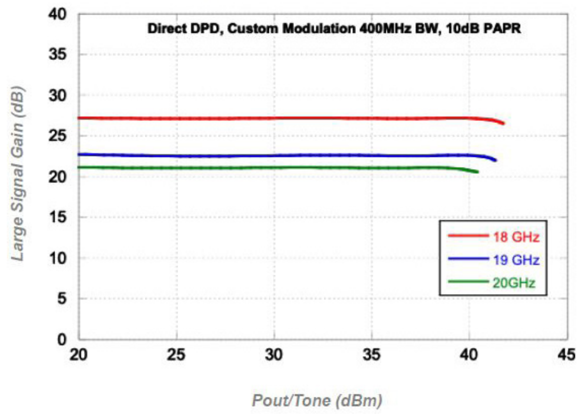
Application Notes

It is typical for GaN HPAs to exhibit a soft compression characteristic as can be seen on the AM/AM plot. This can have a detrimental impact on some modulation schemes particularly where a high PAPR is used. Modern digital techniques such as Digital Pre-Distortion (DPD) can be applied to an input signal to linearize the performance and achieve significant improvements on the EVM. By applying DPD to HPA11201721QF it is possible to linearize the HPA. The subsequent graphs of AM/AM and AM/PM show linear performance beyond 40dBm output power. The measurement uses Direct DPD over a signal bandwidth of 400 MHz and 10 dB PAPR.

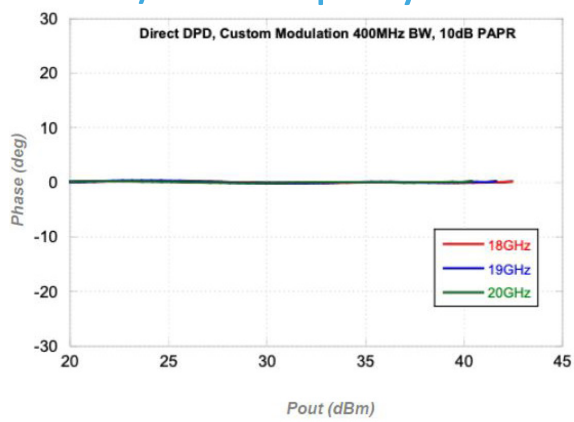
DPD Implementation Process Curves

V_D=25 V, I_{DQ}=300 mA, V_G~-3.6 V typical, T_A=25 °C

AM/AM vs Frequency



AM/PM vs Frequency



Frequency	18	19	20	GHz
Signal Bandwidth	400	400	400	MHz
EVM	1.6	1.6	0.9	%
Pin (avg)	5.2	8.8	8.8	dBm
Pout (avg)	33.6	32.4	31	dBm
Pout (max)	42.1	42.0	40.6	dBm
Gain	28.4	23.6	22.2	dB
Crest Factor	10	10	10	dB

Contact Information

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